THE CLAIMS

1. A packaged semiconductor chip designed for operation throughout a predetermined range of ambient temperature, comprising:

a metal carrier possessing a first coefficient of thermal expansion;

a semiconductor chip, said semiconductor chip containing upper and lower surfaces and including at least one integrated circuit on said upper surface and a plurality of via bonding pads on said upper surface, and a plurality of vias extending from said lower surface through the thickness of said semiconductor chip to respective ones of said via bonding pads, said semiconductor chip possessing a second coefficient of thermal expansion different from said first coefficient of thermal expansion;

a back metal layer attached to said lower surface of said semiconductor chip, said back metal layer being thin relative to the thickness of said semiconductor chip;

a stress relief buffer for absorbing any strain produced by differences in thermal expansion between said semiconductor chip and said metal carrier due to changes in ambient temperature within said predetermined range of temperature, said stress relief buffer attached to and covering said back metal layer;

an electrically conductive bonding layer attached to and covering said stress relief buffer for bonding said metal carrier to said stress relief buffer;

said stress relief buffer including a plurality of vias, said vias extending from contact with said electrically conductive bonding layer through the thickness of said stress relief buffer and into contact with said back metal layer;

said stress relief buffer having a third coefficient of thermal expansion and a low modulus of elasticity, said third coefficient of thermal expansion being of a value nearer to that of said second coefficient of thermal expansion than to said first coefficient of thermal expansion, whereby strain produced by difference in thermal expansion between said semiconductor and said metal carrier is absorbed in said stress relief buffer;

said stress relief buffer comprising an electrically non-conductive chemically etchable polymer.

2. The packaged semiconductor chip as defined in claim 1, further comprising: a protective layer of dielectric material attached to and covering said upper surface of said semiconductor chip for protecting said upper surface, including said integrated circuit and bonding pads, from particle contamination and emulate a hermetic seal of said semiconductor chip.

3. The packaged semiconductor chip as defined in claim 2, wherein said semiconductor chip comprises any of gallium arsenide and indium phosphide, said back metal comprises a layer of gold, said carrier metal comprises aluminum, and said polymer comprises one of the group consisting of polyimide and parylene.

4. The packaged semiconductor chip as defined in claim 1, wherein said polymer comprises paraylene.

5. The packaged semiconductor chip as defined in claim 1, wherein said polymer comprises polyimide.

6. The packaged semiconductor wafer as defined in claim 1, wherein said back metal (9) of the chip comprises a thickness of five microns, said conductive bonding layer (17) comprises a thickness of about three to six mils, said chip (3) comprises a thickness of between 2 and 10 mils, exclusive of said back metal, and said polymer (13) comprises a thickness of about two to eight microns.

7. The packaged semiconductor wafer as defined in claim 2, wherein said back metal (9) of the chip comprises a thickness of five microns, said conductive bonding layer (17) comprises a thickness of about three to six mils, said chip (3) comprises a thickness of between 2 and 10 mils, exclusive of said back metal, said polymer (13) comprises a thickness of about two to eight microns, and said protective layer (19) comprises a thickness of about two to eight microns .

8. A packaged semiconductor chip designed for operation throughout a predetermined range of ambient temperature, comprising:

a metal carrier possessing a first coefficient of thermal expansion;

a semiconductor chip, said semiconductor chip including a layer of semiconductor material, containing upper and lower surfaces; said layer of semiconductor material including at least one integrated circuit, a plurality of via bonding pads on said upper surface, and a plurality of vias extending from said lower surface through the thickness of said layer of semiconductor material to respective ones of said via bonding pads, said semiconductor chip possessing a second coefficient of thermal expansion different from said first coefficient of thermal expansion;

a back metal layer attached to said lower surface of said layer of semiconductor material, said back metal layer being thin relative to the thickness of said layer of semiconductor material;

a stress relief buffer, said stress relief buffer being electrically non-conductive and being attached to and covering said back metal layer and for absorbing any strain produced by differences in thermal expansion between said semiconductor chip and said metal carrier due to changes in ambient temperature within said predetermined range of temperature;

an electrically conductive bonding layer attached to and covering said stress relief buffer for bonding said metal carrier to said stress relief buffer;

said stress relief buffer including a plurality of vias, said vias extending from contact with said electrically conductive bonding layer through the thickness of said stress relief buffer and into contact with said back metal layer;

said stress relief buffer for absorbing strain produced between said semiconductor and said metal carrier due to a difference in thermal expansion or contraction resulting from a change of temperature within said predetermined range of temperature, said stress relief buffer having a third coefficient of thermal expansion and a low modulus of elasticity, said third coefficient of thermal expansion being of a value more near in value to that of said second coefficient of thermal expansion than to said first coefficient of thermal expansion.